REMARKS

The Applicant respectfully requests further examination and reconsideration in view of the comments set forth below. Within the Office Action, claims 1, 4-6, 9, 10 and 21-28 have been rejected. Accordingly, claims 1, 4-6, 9, 10, and 21-28 are pending.

I. THE FINAL OFFICE ACTION FAILS TO CONSIDER ARGUMENTS ASSERTED IN THE RESPONSE FILED MAY 19, 2004.

Under M.P.E.P. § 707.07(f), an examiner should consider **all** arguments an applicant raises in traversing a rejection. Under § 707.07(f), if an applicant asserts that his invention has advantages over the prior art but the examiner believes that those advantages are not sufficient to overcome a rejection, the examiner should state in the record the reasons for his position. "By doing so the applicant will know that the asserted advantages have actually been considered by the examiner and, if appeal is taken, the Board of Patent Appeals and Interferences will also be advised." *Id.*

As part of its accompanying text, § 707.07(f) cites *In re Herrmann*, 261 F.2d 598 (C.C.P.A. 1958), a case that is directly on point here. In *In re Herrmann*, the Court of Customs and Patent Appeals reversed a rejection of claims for which the applicant had stated advantages. The CCPA found that it was "constrained" to accept the advantages argued by the applicant since they were not challenged by either the examiner or the Board of Appeals. 261 F.2d at 600. The CCPA thus was obliged to allow the claims at issue.

As described below, the final Office Action does not challenge, let alone even address, the Applicant's arguments raised in its *Amendment and Response to Office Action Mailed on February 19, 2004*, which was mailed on May 19, 2004 (the May 2004 Response). In the May 2004 Response, the Applicants explained that the structures recited in its claims have advantages over the cited prior art. Specifically, the final Office Action does not challenge the Applicant's assertions that its invention differs from and has advantages over the bird's beak structure disclosed in the prior art. For at least these reasons, the independent claim 23 and its dependent claims 24 and 25, and the independent claim 26 and its dependent claims 27 and 28 are all allowable. Nor does the final Office Action challenge the Applicant's assertions in the May 2004 Response that embodiments of its invention advantageously have a single device layer that has both an active region and an STI isolation structure. For at least these reasons, the independent claim 18 and its dependent claims 21 and 22 are also all allowable.

II. REJECTIONS UNDER 35 U.S.C. § 103(a)

Within the Office Action, claims 1, 4-6, 9, 10 and 21-28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 5,605,853 to Yoo *et al.* ("Yoo") in view of U.S. Patent Number 5,679,559 to Mehta ("Mehta"). The Applicant respectfully traverses these rejections.

A. Yoo does not teach a structure having (1) a single device layer as taught in the present invention, or (2) an isolation structure with relative depths as taught in the present invention, or (3) both a LOCOS isolation structure and an STI isolation structure.

Yoo is directed to "[a]n integrated process for forming a 4T SRAM and a floating gate memory, with logic, on the same integrated circuit." [Yoo, Abstract] In Figure 7, Yoo discloses an SRAM region 50 formed over a substrate 10 and isolated by a field oxide region 12. The field oxide region 12 is formed below a gate electrode 16 and contacts 28. An active region 22 is formed in a second device layer, the substrate 10. **As stated at page 5 of the May 2004 Response**:

> The SRAM region 50 is thus not formed over a single device layer that comprises a first active region and an STI isolation structure. The isolation structure 12 has an inner portion at a first depth and an outer portion at a second depth, less than the first depth. The isolation structure thus narrows at its edges, having what is called a bird's beak shape.

In accordance with the method, Yoo teaches forming an SRAM, a floating gate memory, and a logic device on the same integrated circuit. Specifically, Yoo teaches a method of forming simultaneously an SRAM and an EEPROM on the same integrated circuit, using a LOCOS isolation process. [Yoo, col. 3, lines 51-55]. Yoo teaches a method of forming a plurality of field isolation regions using a LOCOS isolation process. [Yoo, col. 3, line 55-60] The structure disclosed in Figure 7 of Yoo comprises an SRAM 50 and a gate memory 70 separated by field oxidation regions 12.

Yoo does not teach or suggest that an SRAM and an EEPROM can be formed on the same IC, using a shallow trench isolation (STI) process. Neither does Yoo teach or suggest that an SRAM and an EEPROM can be formed on the same IC, using a combination of a LOCOS and an STI isolation process. As indicated by Yoo, in column 2, lines 18-26, a combination of an SRAM and EEPROM on the same IC is desirable. *However, Yoo specifically teaches that such*

an IC is difficult to fabricate because of the difference in fabrication processes. [Yoo, column 2, lines 23-26] In column 2, lines 18-26, Yoo states:

> It may be also desirable to form more than one type of memory structure on the same IC, such as an SRAM in conjunction with an EEPROM (Electrically Erasable Programmable Read Only Memory), as well as logic devices. However, such an IC is difficult to fabricate due to the difference in the typical processes for forming memory and logic and for forming significantly different memory devices.

This statement suggests that Yoo's invention is directed to a method of combining an SRAM and an EEPROM on the same IC, when the same LOCOS isolation process is used on all the regions of the substrate. By this statement, Yoo further concedes that his method does not solve the difficulty of fabricating an SRAM and an EEPROM on the same substrate. Rather, Yoo suggests that an alternative to finding a method of combining two methods would be to improve the current LOCOS isolation method so as to be used on both the SRAM and EEPROM. Further, Yoo teaches away from using multiple different isolation processes on a single IC. Yoo acknowledges the inherent difficulty of applying multiple different isolation processes on an IC, and does not suggest or teach applying a LOCOS and STI isolation process on the same substrate.

B. Mehta does not teach a structure having (1) a single device layer as taught in the present invention, or (2) an isolation structure with relative depths as taught in the present invention, or (3) both a LOCOS isolation structure and an STI isolation structure.

Mehta teaches a device and method for isolating regions of a circuit device in a semiconductor substrate. The method comprises the following steps: forming a first insulation region and a second insulation region; etching a trench in the first insulation region, the trench extending into the semiconductor substrate to a depth below the surface of the substrate; filling the first isolation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of the substrate; and thermally growing a field oxide in the first and second isolation regions. [Mehta, Abstract and col. 4, line 46 to col. 6, line 49]

In Figure 18, Mehta discloses a structure formed in accordance with the method. Figure 18 discloses a substrate 100 containing a first trench 242 and a second trench 240, isolated from each other by a thin layer of oxide (unnumbered). **As stated at pages 6-7 of the May 2004**

Response:

> The portions used to isolate and form the active regions are thus formed from multiple device layers. The first trench 242 has a center portion at a first depth and an outer portion at a second depth, less than the first depth. The first depth thus has a classic bird's beak shape. The disadvantages of bird's beaks are well known in the art, and at column 6, lines 34-41, Mehta teaches an embodiment for minimizing the negative effects of a bird's beak: "Partial nitride encapsulation is shown in FIG. 18; total nitride encapsulation occurs if spacers 180 are not etched back. No nitride encapsulation occurs if the spacers are etched off completely. Nitride encapsulation tends to reduce the bird's beak effect which is commonly seen in LOCOS processes."
>
> Mehta further teaches at column 7, lines 8-13: "Significant encroachment or ΔW of the bird's beak region can reduce the effective area of the active region between the isolation areas. By incorporating nitride encapsulation in conjunction with the method and structure of the present invention, encroachment can be reduced." As described below, embodiments of the present invention provide a structure that advantageously do not have a bird's beak and thus do not need to rely on nitride encapsulation or other additional isolation techniques.

Mehta does not teach or suggest combining a LOCOS isolation structure and an STI isolation structure. Instead, Mehta teaches a LOCOS region and a field oxidized trench region (*see, e.g.*, Mehta, col. 6, lines 21-22), not an STI region. At column 7, lines 42-25, Mehta makes clear that it does not teach STI: "Finally, in shallow trench isolation, a critical planarization mask is generally needed to reduce such dishing. *In the present method and apparatus*, no such critical mask is needed" (italics added).

Still, at page 3 of the final Office Action, it is stated that "Furthermore, the trench isolation is needed in densely packed regions where the active spacing is small, such as a memory array in a DRAM, SRAM, or EEPROM; see [Mehta] also, col. 4, lines 50-56." This is simply not true. Densely packed regions often rely on other isolation structures. And while other isolation structures are used, none combine STI and LOCOS as taught in the present invention.

C. There is no motivation to combine Mehta and Yoo because Mehta teaches against STI.

The M.P.E.P. makes clear that "[i]t is improper to combine references [to support a § 103 rejection] where the references teach away from the combination." M.P.E.P. § 2145(X)(D)(2) (Feb. 2003) (citing *In re Grasselli*, 713 F.2d 731, 743 (Fed. Cir. 1983)). The case against a § 103

rejection is even stronger here, where neither Yoo nor Mehta even teaches an STI structure. Indeed, Mehta teaches against using STI structures in general. For example, at column 2, lines 50-58, Mehta states:

> However, shallow trench isolation (STI) is relatively complex because an anisotropic etch must be used to define the trench, the trench must be etched deeply into the silicon, and filling the trench with the isolation material can raise additional processing issues in preparing the integrated circuit. STI also results in relatively sharp corners at the edges of the trench at the silicon surface. This can result in electrical field leakage at these corners and gate oxide quality problems.

In the Summary of the Invention, Mehta states that one "object of the invention is to provide a process which provides significant advantages over shallow trench isolation and combination of shallow trench isolation and local oxidation processes." [Mehta, col. 3, lines 56-59] Later, Mehta states that "[STI] technology . . is replete with problems." [*Id.*, col. 7, lines 21-22]

Mehta distinguishes its invention over STI, and thus teaches way from STI, by stating that its invention "preserves the familiar and well-characterized interface between active regions and isolation regions in the LOCOS field. No edge oxide quality problems would therefore result." [*Id.*, lines 26-29] Mehta further states that "[STI] is subject to trench corner leakage" (*id.*, line 30-31) and produces "dishing [which causes] thinning of the isolation in wide-trench regions" (*id.*, lines 38-39). Thus, Mehta teaches away from structures that use STI structures alone or in combination with any other isolation structures.

D. The final Office Action improperly finds motivation to combine Mehta and Yoo.

Within the final Office Action, it is concluded that it would have been obvious to use the STI isolation technique as taught by Mehta in the substrate of Yoo. Specifically, it is stated within the final Office Action, "[I]t would have been obvious to one of ordinary skill in the art at the time of the invention was made to use STI isolation technique as taught by Mehta in Yoo et al. substrate in order to scale the minimum spacing between regions." The Applicant respectfully disagrees with this conclusion.

As discussed above, Mehta teaches away from the use of STI. Further, to support this conclusion, a *prima facie* case of obviousness must be demonstrated. No such demonstration has been made here. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation demonstrated, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine

the teachings of the references. Second, there must be a demonstration that the combination of the prior art references would result in a reasonable expectation of success. Third, the combination of the prior art references must teach or suggest all the claim limitations. [M.P.E.P § 2142 - 43.]

First, there is no suggestion or motivation to combine Yoo and Mehta. Yoo teaches away from including an SRAM and an EEPROM on the same IC, isolated by a combination of a LOCOS and a second isolation technique. Furthermore, Mehta does not teach or otherwise indicate that the first and second isolation techniques can be applied to isolate an SRAM and an EEPROM on a common IC. Therefore, it would not have been obvious to one skilled in the art to combine the teachings of Yoo and Mehta. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). Within the Office Action, there has not been any reference to any teaching, hint or suggestion in either Yoo or Mehta suggesting the desirability of combining these two references.

Further, there is no indication in the prior art that a combination of Yoo and Mehta would result in a reasonable expectation of success. As indicated by Yoo, in column 2, lines 18-26, a combination of an SRAM and EEPROM on the same IC is desirable. *However, Yoo specifically teaches that such an IC is difficult to fabricate because of the difference in fabrication processes.* [Yoo, column 2, lines 23-26] Furthermore, the teachings of Mehta do not indicate or suggest that the first and second isolation techniques can be applied to isolate an SRAM and an EPROM on a common IC. The combination of the teachings of Yoo and Mehta would not have resulted in a reasonable expectation of success. Therefore, the combination of the teachings of Yoo and Mehta does not render the current invention obvious.

Even if considered proper, the combination of Yoo and Mehta does not teach the claimed invention. In contrast to the teachings of Mehta, Yoo and their combination, the present invention teaches a system for *independently* or *non-concurrently* integrating SRAM cells and flash EPROM cells onto a single silicon substrate. As discussed above, neither Mehta, nor Yoo, nor their combination teaches or suggests forming an SRAM and an EPROM on a single substrate using a combination of a LOCOS isolation process and an STI isolation process. In column 2, lines 18-26, Yoo states the following:

> It may be also desirable to form more than one type of memory structure on the same IC, such as an SRAM in conjunction with an EEPROM (Electrically Erasable Programmable Read Only Memory), as well as logic devices. However, such an IC is difficult to fabricate due to the difference in the typical processes for forming memory and logic and for forming significantly different memory devices.

This statement suggests that Yoo's invention is directed to a method of combining an SRAM and an EEPROM on the same IC, when the same LOCOS isolation process is used on all the regions of the substrate. By this statement, Yoo further concedes that his method does not solve the difficulty of fabricating an SRAM and an EPROM on the same substrate. Rather, Yoo suggests that an alternative to finding a method of combining two methods would be to improve the current LOCOS isolation method so as to be used on both the SRAM and EEPROM. Therefore, it would not have been obvious to one skilled in the art, that Yoo could have been combined with Mehta to disclose the current invention. Further, Yoo appears to be teaching away from using multiple different isolation processes on a single IC. Yoo acknowledges the inherent difficulty of applying multiple different isolation processes on an IC, and does not suggest or teach applying a LOCOS and STI isolation process on the same substrate. Therefore it would not have been obvious to one skilled in the art from the teachings of Yoo, that a LOCOS and STI isolation process could have been used to form an SRAM and an EEPROM on a common substrate. Further, as discussed above, Mehta teaches away from the use of the STI isolation technique. Accordingly, neither Yoo, nor Mehta, nor their combination teaches or suggests a common substrate having an SRAM device isolated by an STI isolation structure and a Flash EPROM device isolated by a LOCOS isolation structure.

E. The present invention comprises a structure different from that disclosed in both Mehta and Yoo.

The present invention is directed to semiconductor devices and systems comprising an SRAM device and an EPROM device on a single substrate. The SRAM device is formed on an STI isolation structure and the EPROM device is formed on a LOCOS isolation structure. The present invention thus provides on a single substrate both low-voltage devices and high-voltage devices. Such a structure has the advantages of smaller package size, less interference, and quicker transmission of data between the SRAM and EPROM cells. [Specification, page 10, line 24, to page 11, line 4]

F. The claims distinguish over the prior art.

1. Claims 1 and 4

The independent claim 1 is directed to a semiconductor device. The semiconductor device of claim 1 comprises a common substrate, an SRAM device implemented on the common substrate and isolated by an STI isolation structure, and a flash EPROM device implemented on the common substrate and isolated by a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently. As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests a common substrate having an SRAM device isolated by an STI isolation structure and a flash EPROM device isolated by a LOCOS isolation structure. Within the Office Action it is stated that "Mehta discloses the first [isolation] technique is the STI technique and the second isolation technique is LOCOS isolation, as discussed in claim 1." The Applicant respectfully disagrees with this statement. Instead, Mehta teaches a LOCOS region and a field oxidized trench region. As discussed above, Mehta teaches away from using an STI isolation structure. For at least these reasons, claim 1 is allowable over the teachings of Yoo, Mehta and their combination.

Within the final Office Action, the limitation in claim 1 reciting "wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently" is characterized as a process limitation. Within the final Office Action, it is then stated that this language would carry no patentable weight.

While not agreeing with this characterization of the claim language as a process limitation, the Applicants contend that even if it were true, claim 1 recites additional structure that distinguishes it over the prior art. Thus, even accepting the characterization as accurate, claim 1 is still allowable over the cited references.

Claim 4 is dependent on the independent claim 1. As discussed above, claim 1 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claim 4 is also allowable as being dependent on an allowable base claim.

2. Claims 5 and 6

The independent claim 5 is directed to a system containing different types of isolation structures. The system of claim 5 comprises a common substrate having a first portion including an STI isolation structure and a second portion including a LOCOS isolation structure, wherein

the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently, an SRAM device on the first portion of the substrate, and a flash EPROM device on the second portion of the substrate. As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests a common substrate having an SRAM device isolated by an STI isolation structure and a flash EPROM device isolated by a LOCOS isolation structure. For at least these reasons, claim 5 is allowable over the teachings of Yoo, Mehta and their combination.

Within the final Office Action, the limitation in claim 5 reciting "wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently" is characterized as a process limitation. Within the final Office Action, it is then stated that this language would carry no patentable weight.

While not agreeing with this characterization of the claim language as a process limitation, the Applicants contend that even if it were true, claim 5 recites additional structure that distinguishes it over the prior art. Thus, even accepting the characterization as accurate, claim 5 is still allowable over the cited references.

Claim 6 is dependent on the independent claim 5. As discussed above, claim 5 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claim 6 is also allowable as being dependent on an allowable case claim.

3. Claims 9 and 10

The independent claim 9 is directed to a semiconductor device. The semiconductor device of claim 9 comprises a common substrate having a first portion including an STI isolation structure and a second portion including a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently, an SRAM device implemented on the first portion of the substrate, and a flash EPROM device implemented on the second portion of the substrate. As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests a common substrate having a first portion with an STI isolation structure and a second portion with a LOCOS isolation structure. For at least these reasons, claim 9 is allowable over the teachings of Yoo, Mehta and their combination.

Within the final Office Action, the limitation in claim 9 reciting "wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently" is characterized as a process limitation. Within the final Office Action, it is then stated that this language would carry no patentable weight.

While not agreeing with this characterization of the claim language as a process limitation, the Applicants contend that even if it were true, claim 9 recites additional structure that distinguishes it over the prior art. Thus, even accepting the characterization as accurate, claim 5 is still allowable over the cited references.

Claim 10 is dependent on the independent claim 9. As discussed above, claim 9 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claim 10 is also allowable as being dependent on an allowable case claim.

4. Claims 18, 21, and 22

The independent claim 18 is directed to a semiconductor device. The semiconductor device of claim 18 comprises a common substrate, a first portion formed on the common substrate, and a second portion formed on the common substrate. The first portion comprises an SRAM device *over a first single device layer.* The first single device layer comprises a first active region and an STI isolation structure. The second portion comprises a flash EPROM device *over a second single device layer.* The second single device layer comprises a second active region and a LOCOS isolation structure.

As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests an SRAM device over *a single device layer* comprising a first active region and an STI isolation structure and a flash EPROM device *over a single device layer* comprising a second active region and a LOCOS isolation structure. For at least these reasons, claim 18 is allowable over Mehta, Yoo, and their combination.

The final Office Action confirms the Applicant's interpretation that the prior art shows the use of multiple device layers where the present invention uses only one. At page 3 of the final Office Action it is stated, "In regard to claims 24 and 27, Mehta or Yoo shows the first structure and second structure are contiguous, see Mehta's fig. 18." Thus, within the final Office Action, one isolation structure comprises the thin layer of oxide, discussed above, a separate layer. Such a structure differs from that recited in claim 18.

a. The final Office Action does not challenge or even respond to the assertions in a previous Amendment and Response that the present invention distinguishes over the multiple device layer in the prior art.

At page 11 of the May 2004 Response, the Applicant pointed out the use of multiple device layers in the prior art. At page 5, the Applicant argued that Yoo disclosed using multiple device layers to form an isolation structure and an active region, and at page 6 he argued that Mehta did the same. In the May 2004 Response the Applicant further explained that the claims in the present invention recite structure different from the prior art. The final Office Action did not challenge let alone respond to these discussions. Accordingly, under M.P.E.P. § 707.07(f) and controlling case law, the independent claim 18 and its dependent claims 21 and 22 are all allowable.

5. Claims 23-26

a. As to claims 23 and 26, the final Office Action confuses the difference between the first depth and second depth as recited in the claims.

The independent claim 23 is directed to a semiconductor device. The semiconductor device of claim 23 comprises a common substrate, an SRAM device implemented on the common substrate and formed over a first active region on a first isolated structure including an STI isolation structure, and a flash EPROM device implemented on the common substrate and formed over a second active region on a second isolated structure including a LOCOS isolation structure. It is further specified in claim 23 that the second isolated structure has an outer portion extending a first depth into the substrate and an inner portion including the second active region and extending a second depth into the substrate. It is also specified in claim 23 that the first depth is larger than the second depth.

As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests an isolated structure having an outer portion extending a first depth into a substrate and an inner portion including an active region and extending a second depth into the substrate, where the first depth is larger than the second depth. Instead, Mehta discloses portions of two isolation structures each having an inner portion extending a first depth into a substrate and an outer portion extending a second depth into the substrate, where the second depth is larger than the

first depth. Both structures result in a bird's beak. Within the Office Action it is stated that Mehta teaches "the first depth is larger than [the] second depth." Because both isolation structures in Mehta have a bird's beak shape, this characterization of Mehta is true only if the first depth is that of the outer portion. **This labeling of the depths is the opposite of that recited in claim 23.** When referring to the depth of the outer portion in Mehta as the first depth and the depth of the inner portion as the second depth, the same terminology used in claim 23, Mehta discloses a structure in which the first depth is smaller than the second depth. Mehta thus discloses a structure different from that recited in claim 23. Yoo also discloses a bird's beak structure which, for the same reasons given above, differs from the structure recited in claim 23. Accordingly, neither Yoo, nor Mehta, nor their combination teaches an isolated structure having an outer portion extending a first depth into a substrate and an inner portion including an active region and extending a second depth into the substrate, where the first depth is larger than the second depth. For at least these reasons, claim 23 is allowable over Mehta, Yoo, and their combination.

b. The final Office Action does not challenge or even respond to the assertions in a previous Amendment and Response that the present invention distinguishes over the bird's beak structure in the prior art.

At pages 6-7 of the May 2004 Response the Applicant pointed out the existence of a bird's beak in the prior art and the discussion in the prior art about the disadvantages of the bird's beak. In the May 2004 Response the Applicant further explained that the claims in the present invention recite structure different from the prior art. The final Office Action did not challenge let alone respond to these discussions. Accordingly, under M.P.E.P. § 707.07(f) and controlling case law, the claims in the present invention are allowable.

Claims 24 and 25 are both dependent on the independent claim 23. As discussed above, the independent claim 23 is allowable over the teachings of Yoo, Mehta, and their combination. Accordingly, claims 24 and 25 are both also allowable as being dependent on an allowable base claim.

The independent claim 26 is directed to a system containing a semiconductor device having a plurality of isolated structures. The system of claim 26 comprises a common substrate having a first area including an STI isolation structure and a second area including a LOCOS isolation structure, the second area having an outer portion extending a first depth into the

substrate and an inner portion including an active region extending a second depth into the substrate, wherein the first depth is larger than the second depth, an SRAM device implemented on the first area of the substrate and a flash EPROM device implemented on the second area of the substrate.

As discussed above, neither Yoo, nor Mehta, nor their combination teaches or suggests an isolated structure having an outer portion extending a first depth into a substrate and an inner portion containing an active region and extending a second depth into the substrate, where the first depth is larger than the second depth. For at least these reasons, claim 26 is allowable over the teachings of Mehta, Yoo, and their combination.

Claims 27 and 28 are both dependent on the independent claim 26. As discussed above, the independent claim 26 is allowable over the teachings of Yoo, Mehta, and their combination. Accordingly, claims 27 and 28 are both also allowable as being dependent on an allowable base claim.

G. In the "Response to Arguments" section, the final Office Action ignores the teachings of Mehta.

At page 4 of the final Office Action, it is stated (bolding added):

> Applicant further contends that Mehta does not teach STI trench. It should be noted that STI is a b[r]oad term that is used to describe a deep trench in a semiconductor substrate. It is recognizable to one of ordinary skill in the art regardless of how it is made. **A deep trench may be considered as an STI trench.** Mehta provides a way to modifies [sic] the process of making STI trench, for example, avoiding masking. However, Mehta realizes that an STI trench is capable of providing its function as isolation.

The Applicants respectfully disagree with this statement for several reasons. First, as stated at page 3, line 25, of the Specification, STI stands for shallow trench isolation. Contrary to the assertion in the final Office Action, a deep trench may not be considered as an STI trench. Mehta does not teach a modified STI trench at all. Indeed, as described above, Mehta teaches against using an STI trench. At column 4, lines 50-53, Mehta specifically states that "The present invention provides significant advantages over the standard LOCOS process, shallow trench isolation (STI), or the self-aligned LOCOS trench (SALOT) processes."

Within the final Office Action, at pages 3-4, it is further stated:

> [T]he fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See Ex parte Obiaya, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). In this case, Mehta indeed discusses the advantage of using a modified STI trench (deep trench over LOCOS where low MOS spacing is necessary, for example, the area of the substrate. STI type trench provides minimum horizontal space, but deeper than LOCOS.

The Applicant respectfully disagrees with these statements for several reasons. First, and most important, Mehta does not teach a modified STI trench. Mehta teaches away from using an STI trench. Second, the prior art does not teach the present invention. Advantages offered by the Applicant flow from the present invention, not from the prior art.

CONCLUSION

For the reasons given above, the Applicant respectfully submits that the claims are in a condition for allowance, and allowance at an early date would be appreciated. If the Examiner has any questions or comments, the Examiner is encouraged to call the undersigned at (408) 530-9700 to discuss them so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
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Dated: September 20, 2004

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CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

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HAVERSTOCK & OWENS LLP

Date: 9/20/04 By: